REMARKS

Claims 1-14 are pending in this application. By this Amendment, claims 1, 3 and 9 are amended. Reconsideration is respectfully requested in view of the above amendments and the remarks below.

The Office Action rejects claims 1-4, 6, 9, 10, 13 and 14 under 35 U.S.C. §102(e) over Masayuki (U.S. Patent No. 6,693,346); rejects claims 5, 7, 11 and 12 under 35 U.S.C. §103(a) over Masayuki in view of Yang (U.S. Patent No. 6,291,881); and rejects claim 8 under 35 U.S.C. §103(a) over Masayuki in view of Moon (U.S. Patent No. 6,566,739). The rejections are respectfully traversed.

In particular, neither Masayuki, Yang nor Moon, individually or in combination, disclose or suggest forming conductive layers on the semiconductor chip that electrically connect the electrodes and the wiring patterns in a manner such that the conductive layers are disposed on side surfaces of the semiconductor chip, as recited in independent claim 1, and similarly recited in independent claims 3 and 9.

Masayuki discloses in Fig. 5 and at col. 7, lines 7-23, semiconductor chips 4A-F connected by leads 5A-5F. As shown in Fig. 5, the leads are not formed on the semiconductor chips in a manner such that the leads are disposed on side surfaces of the semiconductor chip.

Neither Yang nor Moon compensate for the above-noted deficiencies of Masayuki.

Yang discloses in Fig. 4B that a smaller semiconductor chip 404B is mounted on a larger semiconductor chip 402. Similar to Masayuki, the metal wires 410, which connect bonding pads 408 to pins 400 are not formed on the semiconductor chips in a manner such that the metal wires 410 are disposed on side surfaces of the semiconductor chip.

Moon discloses in Fig. 2 that an upper chip 20 is mounted on a lower chip 10 and connection terminals 71, 81 of the semiconductor chips are bonded to metal patterns 74, 84,

which are bonded to a lead 40. As shown in Fig. 2, the metal patterns 74, 84 are not formed on the semiconductor chips in a manner such that the metal patterns 74, 84 are disposed on side surfaces of the semiconductor chip.

Therefore, independent claims 1, 3 and 9 define patentable subject matter. Claims 2, 4-8 and 10-14 depend on the respective independent claims, and therefore also define patentable subject matter as well as for the other features they recite.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-14 are earnestly solicted.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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